Fast ADC

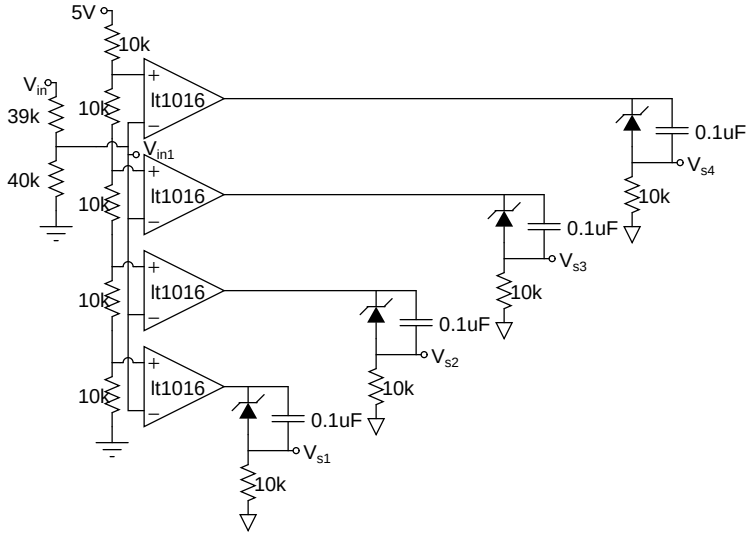
6.331 Design Project 3
Piotr Mitros

May 2002

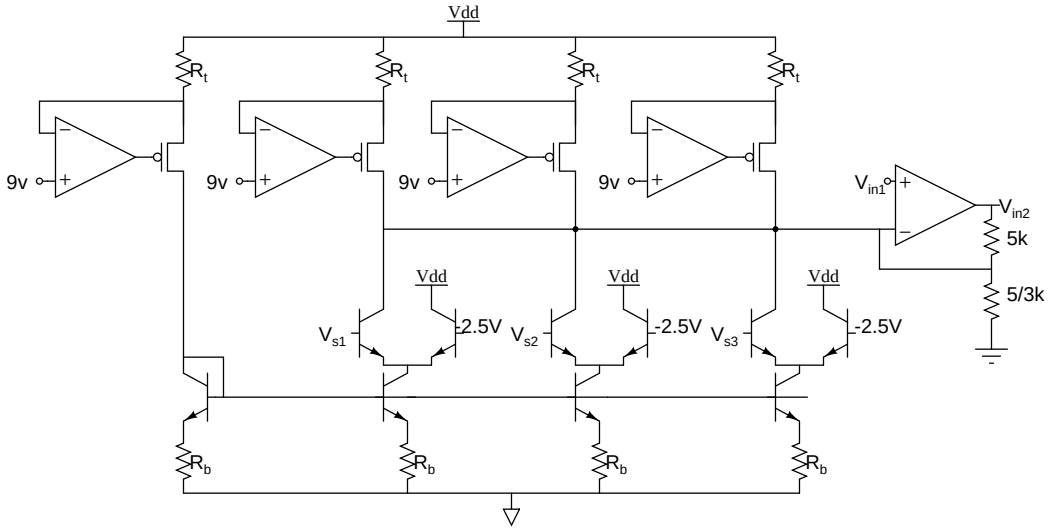
1 Design Overview

We run the input through a 2 bit Flash ADC. We remove the results of the first conversion, and run the remainder through a series of 1 bit ADCs to recover successive bits.

The flash ADC is shown below:

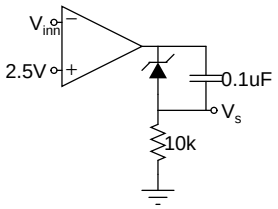


We use this stage to remove the MSB from the input and get a gain of four:

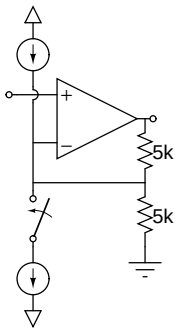


With $R_B = 10k \cdot (1 - \frac{1}{2\beta})$, where β is the minimum β of the transistor used in the differential pair above (∞ if there is no diff pair). We use this to cancel out half of the finite beta effects. R_t is $5k$. The $5/3k$ resistor can be made out of three $5k$s.

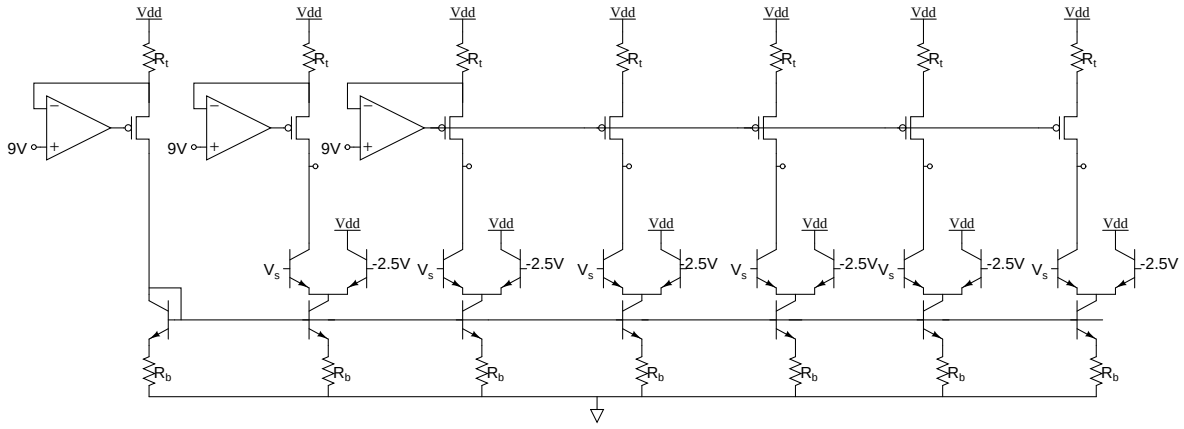
Next, we use the following as a 1 bit DAC:



And this stage to successively remove the next offsets:



And we use this set of current sources for the above stage:

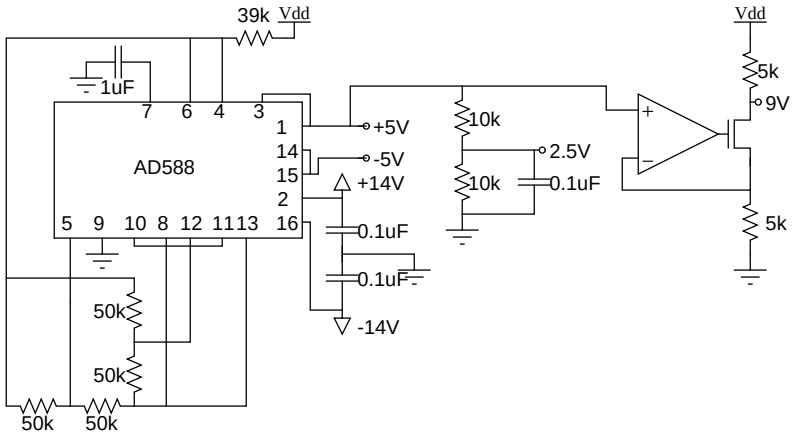


With $R_B = 10k \cdot (1 - \frac{1}{2\beta})$, where β is the minimum β of the transistor used in the differential pair above (∞ if there is no diff pair). R_t is $5k$.

2 Specs

We need to have 8 bits accuracy from 5V, so we are alloted $5V/512 \approx 10mV$ of an error budget.

3 Voltage Reference



Our voltage reference is the Analog Devices AD588KQ. This is accurate to within 1mV before tuning. We scale this down before using (to 0.5mV in most stages).

We use the output voltage to generate a precision current through a resistor that we will then use to generate the remainder of the currents. In the current sources, the AD588 contributes the full 1mV of error. The operational amplifier used is the AD8602A, which contributes at most an additional 0.5mV of error.

These errors do not add; a 1mV error on both the voltage reference and the current reference would still result in 1.5mV total error. As such, the voltage reference contributes a total of $<$ 1.5mV error.

4 Amplify and Offset Stage

In the amplify-and-offset stages, we use OPA642PB operational amplifier. Response time to a 5V step is under 24ns. Offset voltage is 1mV. Distortion contributes negligible error (a few μV). Total delay is under 168ns.

5 Comparators

The LT1016 comparator gives less than 3mV error, and a propagation delay of under 15ns for a small overdrive.

The LT1712 has an offset voltage of less than 5mV, and a propagation delay of under 6ns.

We use the LT1016 for the first 2 bits, and the LT1712 for the last 6. This gives less than 3mV of total error and a delay of 51ns. Note that we do not have to add the comparator errors, since a large error in an MSB would cause all of the remaining LSB comparators to flip in the reverse direction.

6 Current Sources

In the first three current sources (for the two MSBs), we need a fairly high level of precision of current, so we use individual op-amp controlled current sources on top, and a MAT04 supermatched quad for the sources on bottom.

We have a precision current source from the AD8602A operational amplifier, a reference voltage, and a Vishay hermetically sealed ultra-high precision foil resistor. The current error is dominated by the error from the voltage reference (we used a similar setup to achieve 14 bits of accuracy in the DAC), which is calculated in that section, and the 500mV error of the operational amplifier, and finite input current, which adds another 500mV.

The transistors used for the differential pair are the Fairchild 2N3962. Although these are moderately slow devices, we chose them for the high DC current gain of 550-1400. This introduces an error of $(1/550 - 1/1400)/2$, or about 0.05%. Switching time ought to be on the order of 90ns (the 2n3904 switches at about 30ns, and has an f_t three times greater)[1].

The MAT04 supermatched quad gives a current gain match of 2%, with a current gain of over 400, which results in at most a 0.005% error due to finite β. The offset voltage is guaranteed down to $200\mu V$, so with 10V emitter degeneration, we have 0.02% error.

For the remaining bits, we use a similar setup, but with fewer/cheaper/fast/less precise parts.

Here, we use faster, lower β transistors in the mirrors. For the third bit, we still use the 2N3962. For the fourth bit, we use the 2N3904 (switching time of about $30ns$, error of about 0.5%), and finally, we use the KSC2757 in the last four bits (switching time of about $10ns$, but β of only 60, so an error of just under 1%).

[1] We spoke to one of the high-speed DAC groups, who told us that calculations significantly underestimate actual switching speed; we used their experimental values for the 2N3904 and extrapolated.

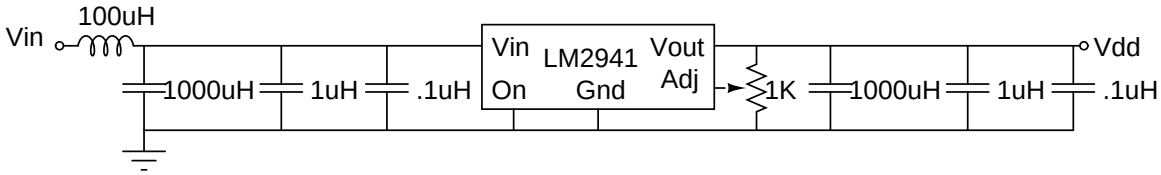
Also, on the least significant bits, we can tolerate large amounts of error, so we just mirror the current over directly, without the precision op-amp approach used in the MSBs.

The MAT04 spec sheet did not give numbers for Early voltage effects. With a reasonable Early voltage, the effects should be negligible because of the amount of emitter degeneration we use. If the effects turn out to be significant, we can eliminate them with a cascode or Wilson current mirror.

The total error from the current sources comes to under 2mV. The total delay is on the order of 250ns.

7 Power Line Filter

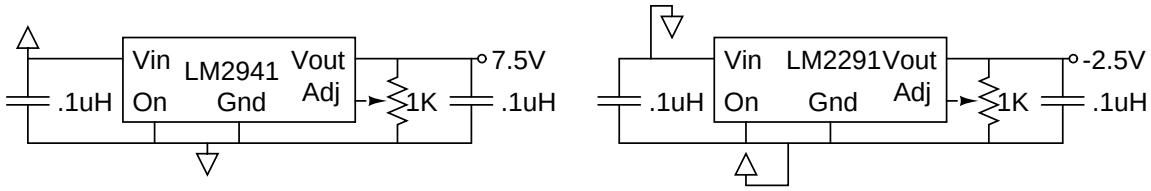
We use an LC low-pass filter followed by a regulator to achieve a stable $14V$ on the power line. This buys us a reduction in power line instability down to $\pm 500\mu V$ from power line fluctuation, and $\pm 2.5mV$ due to to temperature fluctuations, for a total of $\pm 3mV$ power line noise. Although this is not strictly necessary, it means we do not have to worry about power line fluctuations in the rest of the design.



We use an identical circuit for the -14V rail with an LM2291 regulator. This again gives fluctuations of about $3mV$ (though dominated by the lower power supply rejection).

This means that other parts of the circuit only need to reject power supply fluctuations by about 6dB. All of the parts we use have at least several orders of magnitude greater power supply rejection.

We scale this voltage down to make the 7.5V/2.5V rails using another pair of regulators:



8 Construction Details

We have small geometry $0.1\mu F$ ceramic capacitors soldered between the supply pins across the back of every chip in the circuit.

All operational amplifiers and comparators run off of the -2.5V/+7.5V rails. This gives the necessary 0-5V input and output swing. We can use any zener in the 7V range.

9 Conclusion

We demonstrated a ADC topology capable of achieving the specs required. Speed was just under half a microsecond. Total error was about 8.5mV.