Slow DAC

6.331 Design Project 2
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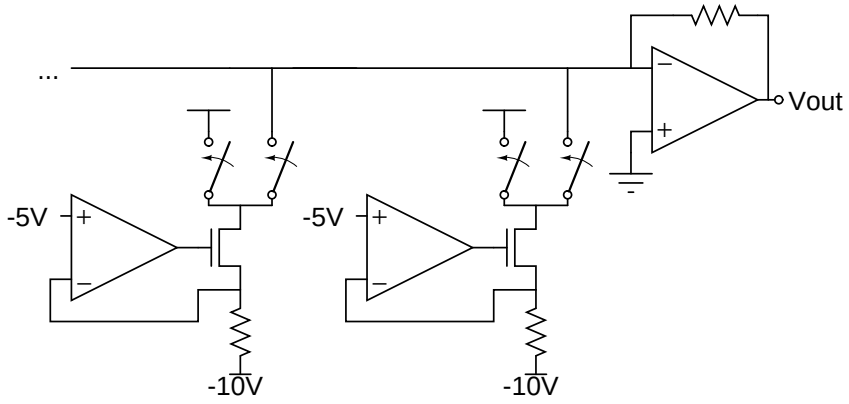
1 Design Overview

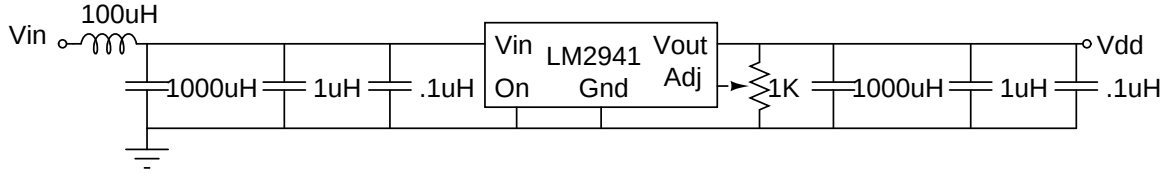
We use a current switching architecture. We run a precision voltage across a series of resistors



To have 14 bits accuracy, we have an error budget of $\frac{5V}{2^{15}} \approx 156\mu V$, or about $30ppm$.

2 Power Line Filter

We use an LC low-pass filter followed by a regulator to achieve a stable $14V$ on the power line. This buys us a reduction in power line instability down to $\pm 500\mu V$ from power line fluctuation, and $\pm 2.5mV$ due to to temperature fluctuations, for a total of $\pm 3mV$ power line noise. Although this is not strictly necessary, it means we do not have to worry about power line fluctuations in the rest of the design.

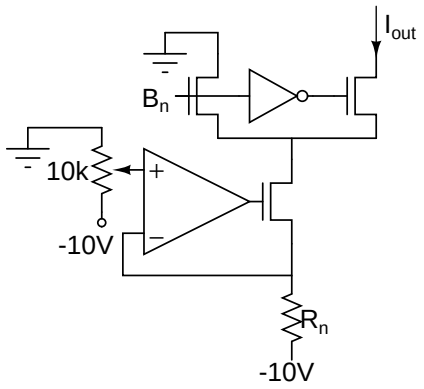


We use an identical circuit for the -14V rail with an LM2291 regulator. This again gives fluctuations of about $3mV$ (though dominated by the lower power supply rejection).

This means that other parts of the circuit only need to reject power supply fluctuations by about $30dB$. All of the parts we use have at least several orders of magnitude greater power supply rejection.

3 Current Source

Each current source is:



Where $R_n = 4K/2^n$, and V_+ is set at around -5V, and trimmed as necessary.

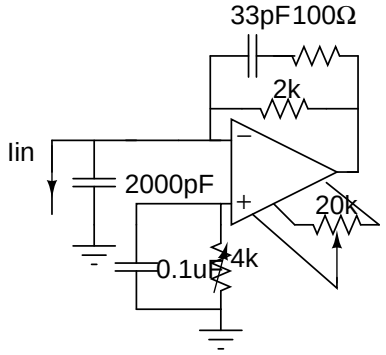
On the current sources, we mostly care about input offset current and voltage drift. As such, we use the AD8610B operational amplifier. This gives a voltage drift of $1\mu V/^oC$, for a total error of $\pm 10\mu V/^oC$ over the temperature range. Since voltage error in the reference of the nth bit only contributes $1/2^n$ error, this corresponds to at most a $20\mu V$ error in the MSB, which translates to about 4ppm.

The amplifier has an input current of $10pA$. Over the 14 bits, this gives a maximum error of $140pA$. This is completely negligible compared to the $25mA$ of full-range current.

The MOSFETs are 2N7000s. The MSB will be running at less than 2/3 of the rated power dissipation. Switching time is about 10-20ns, so negligible compared to the settling time spec. The op amps should also have ample time to cancel out any charge injection.

4 Output buffer

Our output buffer is simply:



Here, we use an AD797B operational amplifier. We can use the 2k pot to trim out constant current error (or other offset errors). This still leaves a painfully large $0.1\mu A$ change in input current over our temperature range. This corresponds to about 4ppm of error.

Each stage has a maximum input voltage drift of $0.6\mu V/^oC$, ($0.2\mu V/^oC$ typical) which gives $6\mu V$ error, or about 1.5ppm.

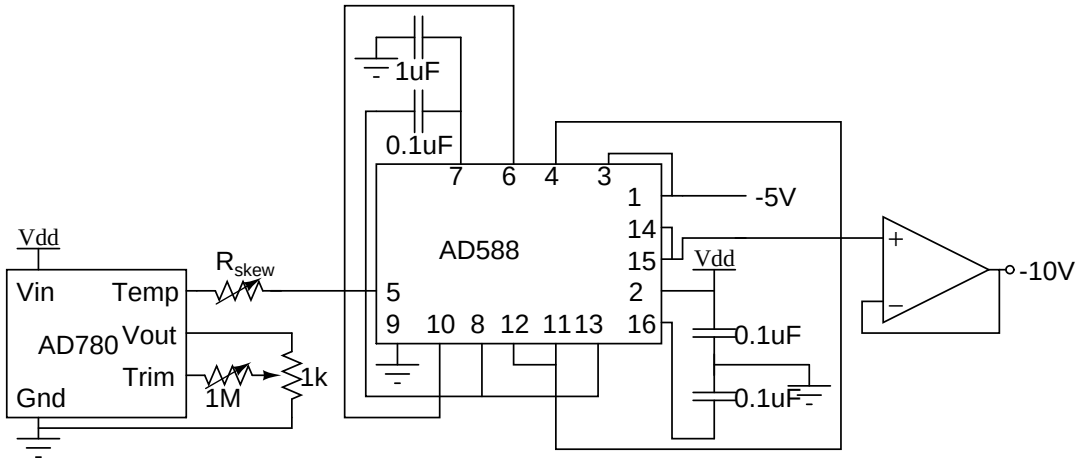
Total harmonic distortion is -120db at 20KHz, or 1ppm.

The AD797B has an output resistance of at most $3m\Omega$. With a $1k$ load, this corresponds to an error of at most $3ppm$.

The 2000pF capacitor shunts any switching transients to ground. The resistor-capacitor network around the 2k is recommended in the spec sheet.

5 Precision Voltage Reference

We use an Analog Devices AD588KQ as a voltage reference. This gives a maximum voltage error of about $1.5ppm/^oC$ ($0.95ppm$ typical). Over a 20^oC range, this would give a maximum error of $15ppm$ ($9.5ppm$ typical), which would be half of our error budget. Fortunately, when we look at the actual performance curve (figure 7), we see that it is very linear over any 20^oC range around 25^oC. As such, we can compensate for it by trimming the gain from an accurate temperature measure, such as that available from the AD780. So our overall temperature reference circuit is:



(Note: All pins left out of schematic are left unconnected).

V_{REF} is used to give the last level of compensation to temperature variations. The crude value depends on R_1, R_2 and R_3 internal to the AD588, whose value is not listed in the spec sheet. As such, the general range will have to be experimentally determined. Depending on whether the temperature coefficient of the AD588 is positive or negative within our operating range, we may also need an inversion on R_{skew}. R_{skew} will slightly throw off the output voltage from the expected $-5V$ and $-10V$, but since we are only relying on the stability of this voltage difference, rather than its absolute value, this does not matter.

This reduces temperature dependence by about an order of magnitude for the original, so it remains within a small fraction of the error budget. We will conservatively mark this

as 3ppm.

We use an AD797B as the output buffer. Although this is probably not the ideal op amp for the application, it only introduces 1.5ppm error (see the analysis in the output stage), is capable of putting out more than enough current, and shows excellent behavior at high loads, so is more than sufficient for the task.

6 Calibration Error

We can calibrate each bit to 5ppm. This gives a total miscalibration of $\Sigma 1/2^n \cdot 5ppm = 5ppm$. To calibrate offset, we tweak the 2k pot on the output stage, and look for the zero crossing. We can do this exactly, since our voltage measure has accuracy in ppm of the voltage we are measuring. We will assume that the trimming of other errors is, very conservatively, down to a total of another 5ppm.

7 Precision Resistors

We use Vishay hermetically sealed ultra-high precision foil resistors. These resistors have a tolerance of .001% and a temperature coefficient of 1 $ppm/^oC$ between 0^oC and 60^oC. This would give an error of $\pm 1ppm$ over the temperature range. Fortunately, our design is ratiometric. Since the resistors match to about a thousandth of a percent, we can assume at least some matching on temperature coefficient. Even with only 5 percent temperature coefficient matching on the resistors, the error injected becomes trivial.

The pots used in each bit stage are Vishay model 533 pots for 1/100th of the voltage, in series with a pair of pots for the remaining 99/100ths (to simplify schematics, we drew this as a single pot). Their temperature coefficient scales to about $.2ppm/^oC$.

8 Settling Time

The settling time spec is completely trivial. The switches take about 10ns to switch. The AD797B on the output settles with 800ns to 16 bit accuracy. The SN54ABT162244 inverter has a switching time of 5.6ns. All other elements, to a first order, only operate at DC. The current source op amps need to compensate for any short switching transients, but that's a very small transient. Our settling time should still be under $1\mu S$.

9 Total Error

Using the conservative estimates for error from above, we get 27.5ppm of error. We are close to, but meet the spec, of 30ppm. In practice, this is a very large overestimate of the error. We used maximum, rather than typical, values for component errors. In general, Analog parts tend to come pretty close to the typical values. We assumed an additional 5ppm trimming error. Also, we added all errors, whereas in reality, some errors will cancel.