A Simple Feedforward Amplifier Topology

6.331 Lab 1
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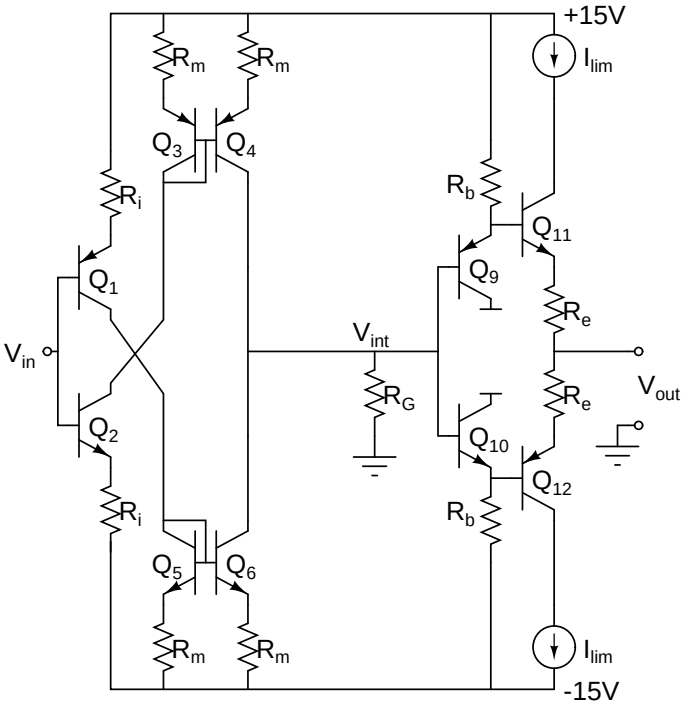
1 Motivation

The United States Patent Office tells us that negative feedback is "another one of those perpetual-motion follies." As such, we chose to design our circuit around a pure feed-forward design.

2 Overview

Our basic design was:



Here, the input transistors Q_1 and Q_2 have a current linearly proportional to V_{in} by a factor of R_i (in addition to a constant bias current). We use a pair of current mirrors (Q_3

through Q_6) to subtract the currents and run them through R_G. The bias currents cancel, whereas the signal currents add, giving a gain of $\frac{2R_G}{R_i}$. We buffer this onto the output node.

3 Circuit Detail

3.1 Input Stage

The circuit contains only one high-impedance node: V_{INT}, which sets the dominant pole. Its frequency depends on parasitic capacitances times R_G.

Since our gain is set by $\frac{R_G}{R_i}$, but our bandwidth is only dependent on R_G, we can theoretically set the two independently. Practically, we run into thermal limits on Q_1/Q_2.

To partially overcome this, we replaced the R_is with a parallel combination of resistor to ground and resistor to rail. This forms a Thevenin equivalent circuit with a low resistance $R_{i,thev}$, but maintains a comparatively low current because of the reduced V_{THEV} across it.

We cannot reduce V_{THEV} too far, as Q_1 and Q_2 would fall into saturation (and we would see some distortion a ways before that). Since $V_{in} = \pm 1V$, we have $V_e = \pm 1.6V$. To be conservative, we set $V_{THEV} = \pm 3V$. Q_1 has a maximum thermal dissipation of $625mW$. With $15V$ across it, and a bit of a safety margin, this gives a maximum current of about $30mA$. R_{THEV} has a maximum voltage of $3.6V$ across it, so we pick $R_{THEV} = 120$.

We reduced the capacitance on V_{INT} by cascoding Q_4 and Q_6 with Q_7 and Q_8, reducing Miller effects in the mirror. We reduced the effects of Q_9 and Q_{10} by using 2N3904 and 2N3906 devices instead of the 2N2905/2N2219 of the rest of our output stage (which would have given better matching), and overcompensated by using 10Ω emitter resistors on the push-pull pair.

The R_ms limit our headroom (in addition to the V_{DSAT} drop across the cascodes). However, if we reduce R_m too far, we would begin have problems with transistor mismatch. We chose values for R_m and V_{casc} that gave the headroom in the specification, but no more. Both of these values could be tweaked further to give more headroom if desired.

We could boost the gain further by having a current gain in the mirror, although we would need to be careful to keep power consumption reasonable.

3.2 Bandwidth Extension

As described so far, the design basically worked, but only achieved a bandwidth of $7.3MHz$. In order to extend this slightly, we added a zero to cancel out the dominant pole. We placed a $200pF$ of bypass capacitance across R_i to give us a little extra boost at high frequencies. This rang a little bit, so to damp it out, we added a 20Ω resistor in series.

This extended our bandwidth to at least $30MHz$. We were not able to measure the exact bandwidth due to equipment limitations.

Note that, given the right impedence, we cancel out the dominant pole exactly. Our gain is $(R_G||Z_{G,parasitic})/(R_{i,top}||R_{i,bottom}||Z_{su})$. It is trivial to see that if we make Z_{su} exactly one tenth of $Z_{G,parasitic}$, the poles and zeros cancel exactly.

Given appropriate test equipment, we could have extended bandwidth further by playing the same trick on Q_4/Q_6 to cancel out the next several poles. With inductors, we could also

potentially inject zeros on Q_3/Q_5. Again, we did not do this, as we had no way of measuring roll-off frequencies beyond the range of the signal generator.

3.3 Output Stage

The output stage uses a standard diamond topology. We chose to implement current limiting by placing a current source in series with Q_{11} and Q_{12}, rather than the more common transistor across R_e to pull off base current. This had the advantage that, at large currents, R_{lim} would take a bit of voltage off of the output transistor.

Perhaps more importantly, this gives a big advantage in terms of construction. In the initial version of the circuit (before using the Thevenin for R_i), every reasonable path between the power rails had either a limiting resistor or current source in the way. This made it very difficult to actually smoke any components. Over the course of the entire project, the only components smoked were:

- Several devices in a series of experiments to determine the feasibility of the design, prior to designing the circuit (looking for things like the distortion on an output stage, etc).
- One fairly late experiment, to determine how the 2N2219/2N2209 parasitic capacitance compared to that of the 2N3904/2N3906. Here, we knew we were going over the thermal limit, and expected to smoke the part beforehand (but collect some useful data in the process)

This had the disadvantage of using a pair of the expensive output devices for each side of the push-pull pair, rather than just one device. We could fix this by using removing Q_{13} and Q_{14} and just relying on $R_{lim} \approx 45\Omega$. R_{lim} and R_{out} would form a practical current limit of $\frac{15V}{R_{lim}+R_{out}}$. At the same time, as we approached this limit, they would give enough of a voltage drop that Q_{11} and Q_{12} ought to be able to withstand shorts to ground.

3.4 Stability

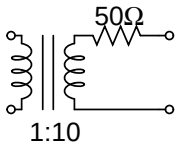
For stability reasons, we added 20Ω resistors on the bases of most transistors. To fix a large $260MHz$ oscillation in the output stage, we added modest collector resistors to Q_9 and Q_{10}.

3.5 Offset

This topology lends itself to a fair amount of DC offset, since any V_{BE} mismatches in Q_1 and Q_2 are amplified by a factor of 10. Fortunately, we can manually fine tune the R_is to eliminate any mismatch should this be an issue, with no impact on performance. In this case, we had no offset spec, so we let them be.

4 Design History

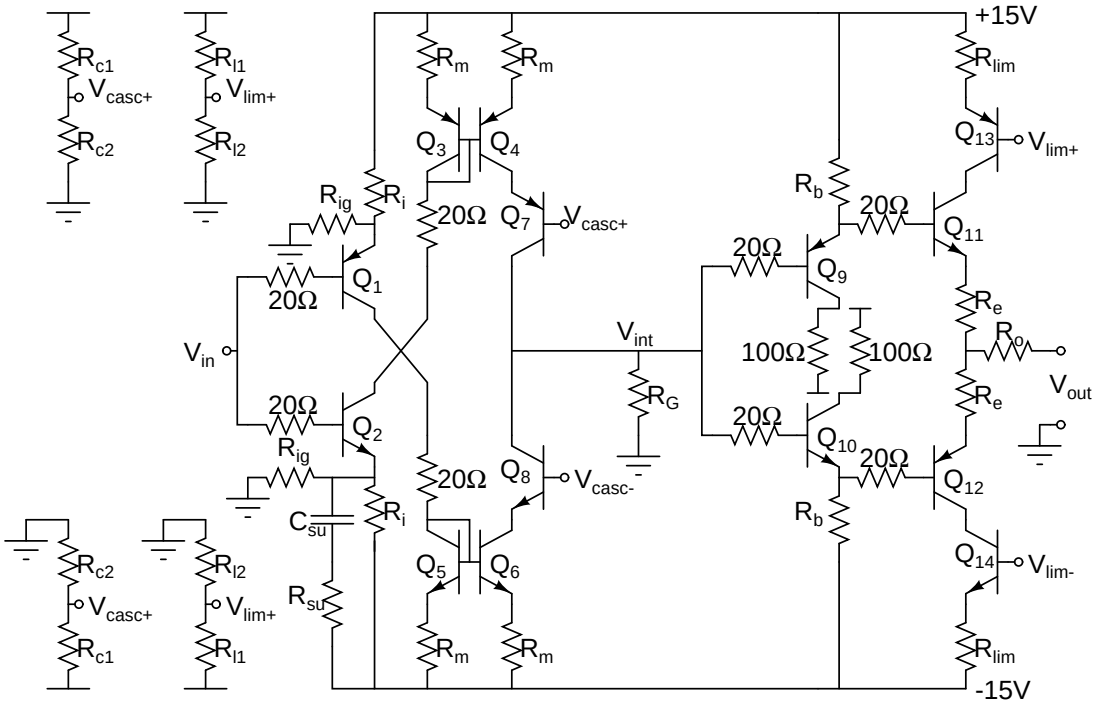
Our initial design consisted of two passive components, and fully met specs:



Our next design was op-amp based, just to have a guaranteed working circuit. We then linearized our output stage to meet the distortion spec, and tried to develop a common-emitter gain stage for it. However, we found that we could not get the headroom desired with a simple common-emitter, so we mirrored the output. For elegance, easy biasing and a free 2× boost in gain, we chose to make this fully differential. At this point, it would make sense to go back to a single-ended design, as we have plenty of bandwidth, but it would save us three transistors.

5 Circuit Detail

The final circuit was:



With component values:
$R_i = 270\Omega + 330\Omega$ (two resistors to split power dissipation)
$R_{ig} = 150\Omega$
$R_m = 47\Omega$
$R_G = 680\Omega$
$R_{lim} = 39\Omega$ (power resistor)
$R_o = 18\Omega + 18\Omega$ (two resistors to split power dissipation)
$R_e = 10\Omega$

$R_{c1} = 3k\Omega$
$R_{c2} = 12k\Omega$
$R_{l1} = 100\Omega$
$R_{l2} = 100\Omega + 120\Omega$ (two resistors for power; not strictly necessary, but convenient not to have to worry about i_{out}/β)
$C_{su} = 100pF + 100pF$ ($120pF$ gap in available values)
$R_{su} = 20\Omega$
$R_b = 1k\Omega$

We built the circuit on the standard 6.331 protoboard. Except in places where it clearly did not make sense (between some base-emitter junctions, near some power supply lines, etc.), every other rail was grounded. For good measure, we placed $0.1\mu F$ caps intermittently between the power rails for high-frequency bypassing. We did not need any low-frequency bypass caps.

6 Results

Our final results were:

Small Signal Bandwidth	Unable to measure; $> 30MHz$
Slew rate	$160V/\mu S$ up, $410V\mu S$ down
Gain	12 unloaded, 6 loaded
Output Swing	$10.5V$
Overshoot to a 1V step	$< 100mV$
Shorts to ground	No problem
Distortion	Looked fine at $10V_{PP}$, $1MHz$

The design can be implemented at a reasonable cost. It uses 10 2N3904/2N3906 transistors and 4 2N2219/2N2095. Given all documented simplifications, this can be brought down to 7/2.

7 Future Improvements

As documented in the text, possible future improvements are:

- Some gain in the current mirror.
- More zeros to stretch out our bandwidth slightly more.
- Removal of Q_7, Q_{13} and Q_{14} for cost savings.
- Bypassing on reference voltages.
- Tweaking R_i to eliminate offset.
- A 300MHz function generator for the lab