6.331 Lab 3

Piotr Mitros

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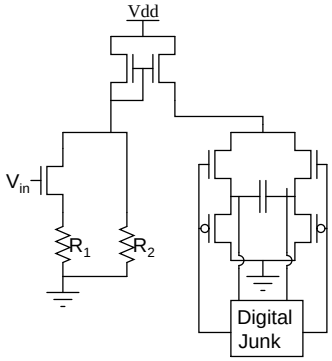
1 Proposed theory of operation for VCO

A block diagram for the VCO is:

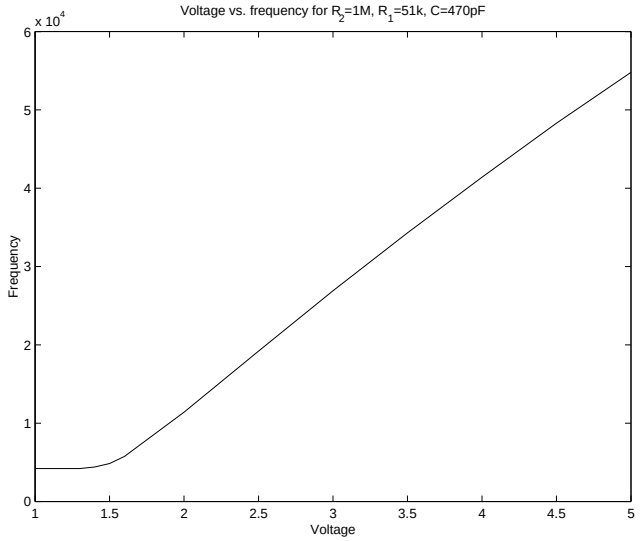


The VCO applies a current to one side of the capacitor. The current is proportional to $V_{DD}/R_2 + V_{IN}/R_1$. When the voltage reaches some switching threshold, the other side of the capacitor charges. As such, we can say:

$$\tau \propto C/\left(\frac{V_+}{R_2} + \frac{V_{IN} - V_{GS}}{R_1}\right)$$

$$f = \frac{1}{2 \cdot \tau}$$

Practically, we found this to match behavior pretty closely. Sweeping V_{IN} gave us:



Changing C scaled frequency fairly linearly (other values as above, with $V_{in} = 1.6V$):

C	f
470pF	5.76 KHz
940pF	3 KHz
1430pF	2.04KHz

Scaling R_1 scaled the slope. As we see with $R_2 = \infty$, $C = 470pF$, $V_{in} = 2.5V$, the behavior is moderately linear (slightly underresponsive to changes in R_1):

R_1	f
51K	38.9KHz
100K	21.9KHz
150K	15.6KHz

Likewise, scaling R_2 scaled the offset ($R_1 = 51k$, $V_{in} = 0$, $C = 470pF$). Again, the response was roughly as excepted, though again, slightly underresponsive:

R_2	f
51K	55.4KHz
100K	32.1KHz
150K	23KHz

Fall and rise time is about 100ns. With a 100pf load, goes up to about 300ns.

2 Phase Comparator II

2.1 Lock limits

Practically, we see several limits on lock range:

- The frequency sweep range of the VCO
- Steady state phase error has to stay under

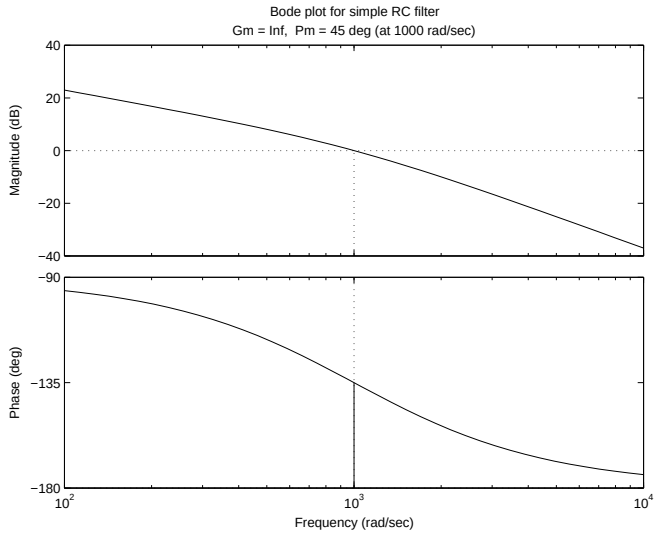
2.2 Simple RC

We have loop transmission:

$$L(s) = K_D \cdot \frac{K_O}{s} \cdot \frac{1}{R_3 C_1 s + 1}$$

So we want to have $R_3 C_1 = 1mS$ for 45^o phase margin at $1krad/s$. We can pick $R_3 = 10k$, $C_1 = 0.1\mu F$. We then have $K_D K_O/(\omega\sqrt{2}) = 1$, for crossover, with $\omega = 1krad/s$ and $K_D = 2.5/2\pi V/rad$. This gives $K_O = 3.55krad/V$, which, holding $C = 470pF$, gives $R_1 = 220K - 240K$. The $220K$ gave $3.6KRad/sec$, while the $240K$ gave $3.3KRad/sec$. We chose the $220k$, which gives slightly more overshoot and bandwidth. To achieve the center frequency of $19KHz$, we pick $R_2 = 240K$. We got $19.2KHz$ at $2.5V$.

This gives us the Bode plot:



To compensate for the slightly larger value of K_o, we cut C_1 down to $0.047\mu F$.

We built the circuit, substituting an LM6152 for the LM310 as the buffer (the LM310 has limited swing when run off of a 5V rail). Center frequency (as defined by zero phase error) was 18.7KHz. We slightly tweaked this with a potentiometer, as overshoot suffered away from the center frequency. Our circuit was able to lock from $15.2 - 23.9KHz$. It seemed to track $15.2 - 26.6KHz$, but somewhat unreliably outside of the lock range. Step response was consistent with the bandwidth and phase margin.

2.3 Lag Loop Filter

We have loop transmission:

$$L(s) = K_D \cdot \frac{K_O}{s} \cdot \frac{R_4 C s + 1}{(R_3 + R_4) C s + 1}$$

We pick $R_1 = 56k\Omega$, $R_2 = 820k\Omega$, $C_1 = 470pF$. This gives $5KHz - 39KHz$ for V_{VCO} of $1V - 4V$ ($1V$ left on each end so we don't hacve to worry about headroom limitations), center

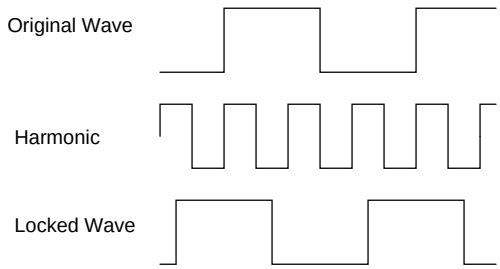
frequency of 18.95KHz, and $K_0 = 14.3KHz/V$. From there, to give our capture range, we just need to keep our phase shift small enough that the phase comparator can still compare. We used a $0.0022\mu F$ cap to get rid of some of the high frequency junk. There was still a bit of ripple left, but it was now manageable.

By calculation and Matlab, we chose $R_3 = 160K$, $R_4 = 10K$, $C = 0.1\mu F$. This gave just over the desired bandwidth and phase margin. In practice, we found we were very slightly under the phase margin spec, and a good bit over the bandwidth spec, so we increased R_4 to 20k.

We had an overshoot of 12%. 90% rise time was about $0.5mS$. Bandwidth was $900Hz$. Lock range was $5KHz - 36.6KHz$ and track range was $5KHz - 47.3KHz$.

3 XOR Detector

Theoretically, the circuit should be able to lock onto harmonics. We can see this with these three wave forms (assuming a PLL designed to lock on with a 90^o phase shift):



Both the original wave and the harmonic on the input could generate the locked wave shown on the output. The average value out from the XOR filter would be the same. Given a small phase shift either way, the output of the XOR would change identically for both waveforms. In practice, we had no problems getting the thing to lock onto harmonics.

K_D should just be $5V/(2\pi)$, so twice the previous. This increases our open loop gain.

This gave marginal overshoot (less than 10%) and rise time of $130\mu S$. We had a lock range of $10.4 - 25.8KHz$ and a track range of $5.1 - 47.5KHz$. Measured bandwidth was like 6KHz

Trying to capture on the upper end of that locked onto harmonics. Lock was generally more difficult to aquire than with II. Unlike the previous, this circuit was duty cylce sensitive.

4 Active Filters

We have the loop transfer function:

$$L(s) = K_D \frac{K_O}{s} \cdot \frac{R_3(C_1 + C_2)s + 1}{(R_4C_1) \cdot s \cdot (R_3C_2 s + 1)}$$

With a two-pole rolloff, our crossover would be at $\sqrt{K_D K_O/(R_4C_1)}$. Because of our lead filter, we'll only have a one-pole part of the time, so this may actually move out a little

bit. For our 45^o phase margin, we need to place our crossover between the pole and zero of the lead (exactly at either, we'll get 45^o phase margin, assuming the two are sufficently far apart).

We found values of $C_1 = 0.1\mu F$, $C_2 = 0.0022\mu F$, $R_3 = 13k\Omega$, $R_4 = 100k\Omega$ to give adequate performance.

Since we are using an LM6152 powered off of the 5V rail, we omitted the clipping diodes. R_1, R_2 and C_1 were kept from the previous section.

We had a bandwidth of 870Hz and an overshoot of about 8%. Both tracking and locking were around the full range of the VCO: $5.1KHz - 51.3KHz$. There was no steady-state phase error.

Tracking error: 5KHz deviation, 100Hz carrier gives $15.5V_{PP}$ wave on phase comp output.

5 Linear Phase Detectors and Frequency Synthesis

We wanted a center frequency of 38KHz. Since the linear phase detector generates junk when the inputs are of significantly different frequencies, we wanted a fairly small swing. Having $R_1 = 560K$ and $R_2 = 91k\Omega||1.5M\Omega$ gave us a center frequency of $37.94KHz$ and a swing of $36.6 - 39.7KHz$ (again, for $V = 1 - 4V$). We have $K_O = 1.21KHz/V$. We can derive that $K_D = 0.3/\pi V/rad$. We use the same compensator as in the previous section, but we pull back bandwidth, so $R_3 = 220k\Omega$ and $R_4 = 560k\Omega$.

We had a slight steady-state error ($< 3\mu S$) due to the propagation delays on the parts. In particular, the 4053 gave a $1\mu S$ maximum propagation delay. However, steady-state error due to the control loop was zero. Overshoot drifted a bit with time, so was difficult to measure, but appeared to be under 10%. It was very clearly under 16%. 90% rise time was 1.3mS. Measured bandwidth was 270Hz. We had no visible tracking error; we were not able to drive the FM deviation very high without losing lock or modulation frequency without running into bandwidth limitations. At the limit where it still tracked and looked like a triangle wave, there was no measureable tracking error. Tracking range was $36.7 - 40.9KHz$, and was limited by the VCO range. Locking range was $40.2 - 40.9KHz$.