Sample and Hold Circuit

6.331 Design Project 1
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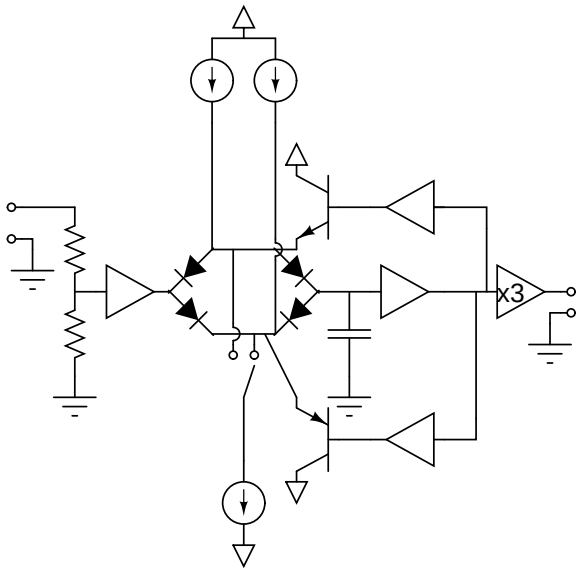
1 Design overview

We use a pretty generic diode switch design:



The only non-standards parts of this design are:

- We run our signal through a voltage divider to attenuate our range from $\pm 10V$ to $\pm 2.5V$. Although this reduces several of our specs by a factor of three, this lets us use $\pm 5V$ operational amplifiers, which can have performances an order of magnitude better than $\pm 15V$ parts. In particular, we can use Burr-Brown operational amplifiers with 0.1 percent settling times of $\approx 20nS$, and bandwidths in the hundreds of megahertz to low gigahertz. This lets us use a significant number of operational amplifiers without much price in speed.
- We use matched diodes on the diode switch to cancel leakage currents

2 OPA640UB Operational Amplifier

2.1 DC Errors

Throughout the circuit, we use the OPA640UB operational amplifier for places where output swing and leakage current are not important. This gives $-75dB$ distortion at $10MHz$. This translates to about 1 part in 1800. Since we are running it at unity gain with an open loop gain of $\approx 1.3GHz/50MHz = 26$ for a $20nS$ sampling time, this reduces to 1 part in 50,000, or completely negligible compared to the $20mV$ spec.

Total operational amplifier noise is $65\mu V$ for a bandwidth of 100Hz up to 500MHz, so is also negligible to our spec.

Slew rate is over $285V/\mu S$, so should not effect circuit operation.

Constant offset will be tuned out, so we don't need to worry about it. Offset drift is $\pm 150\mu V$ over the entire temperature range. This translates to $600\mu V$ input referred offset error.

2.2 Speed

Our settling time to within 0.01 percent is 22nS (0.01 percent translates to about 2mV input referred error for a $\pm 10V$ input, and 1mV for a $\pm 5V$ input).

2.3 Tracking error

We can approximate the transfer function of the open loop operational amplifier as:

$$\frac{a}{1+bs}$$

With $a \approx 200000$, $b \approx a/(1.3GHz \cdot 2\pi)$ cyc/rad. This gives an error function of:

$$1 - \frac{a}{a+1+bs} \approx 1 - \frac{a}{a+bs}$$

So our error coefficients are

$$e_0 = \frac{1}{a+1}$$

$$e_1 = \frac{ab}{(a+1)^2} \approx \frac{b}{a}$$

$$e_2 \approx \frac{b^2}{a^2}$$

And our steady state tracking error is $e_0 + e_1/r_t$. For a $1V/\mu s$ ramp, this translates to about $122\mu V$. For a $10V/ms$ ramp, this translates to something negligible.

3 OPA655 Op Amp

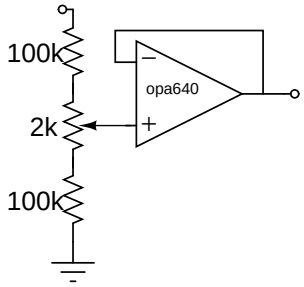
For our buffer in front of the diode switch, we use an OPA655 operational amplifier for it's low ($< 20pA$ at 50^o) input bias current. Following the analysis above, we have:

Error	Absolute	Input-referred
Distortion	-	$632\mu V$
Noise	$60\mu V$	$240\mu V$
Offset Drift	$250\mu V$	$1mV$
Slew Rate	$200V/\mu S$	$800V/\mu S$
Settling Time	$17ns$	$17ns$

Tracking error is unimportant, as this op amp is only used after the sample capacitor. It is negligable for the high-accuracy circuit, and for the high-speed circuit, we have $1\mu s$ for it to settle out.

4 Input Buffer

The input buffer is:

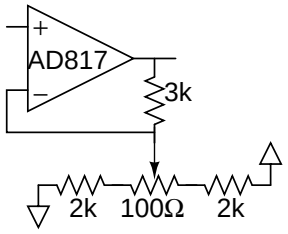


The pot is used to adjust gain. It is 2K so that we can shift it to remove any errors due to the 1k source impedance in the high-speed version.

Analysis of errors is the same as for the OPA640 above.

5 Output Buffer

Our output buffer is:



The pot is used to adjust offset.

6 AD817 Op Amp

Finally, for the output, we need an op amp with a $\pm 10V$ output swing, so we use the AD817. Adjusting our analysis for $1\mu S$ settling time, we have:

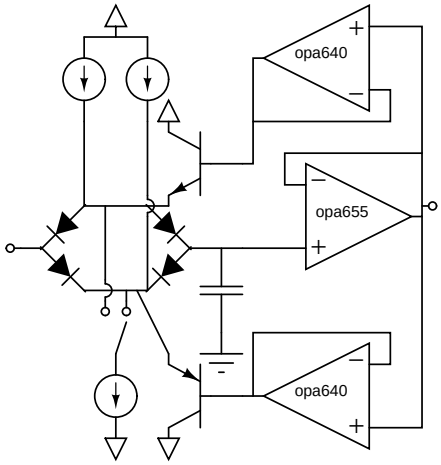
Error	Absolute	Input-referred
Distortion	$22\mu V$	$90\mu V$
Noise	$33\mu V$	$134\mu V$
Offset Drift	$250\mu V$	$1mV$
Slew Rate	$300V/\mu S$	$1200V/\mu S$
Settling Time	$70ns$	$70ns$

Tracking error is unimportant, as this op amp is only used after the sample capacitor. It is negligable for the high-accuracy circuit, and for the high-speed circuit, we have $1\mu s$ for it to settle out.

7 Diode Switch

7.1 Overview

We use a simple 4 diode switch:



The transistors are 2n3904/2n3906 devices, and clip the pull-down voltage to within a V_{BE} drop of the output.

In order to keep temperature reasonable, we use a 30mA bias current through each diode. Although we could construct the switch out of a single BAV99DW diode array, we chose to break it up among two MMBD7000 diode arrays. Although this hurts our offset voltage, it breaks up power dissipation among two lower resistance devices, and so keeps diode temperature (and leakage current) reasonable. Assuming good heat-sinking, which is an automatic side effect of our dead-bug construction technique, junction temperature only increases by $30mA \cdot 1200mV \cdot 357K/W \approx 13^oC$.

Although several other parts offered significantly lower leakage currents (down to 5pA), we chose this one for it's fast $\tau_R = 4nS$. Although this shouldn't matter much, since charge injections tend to cancel, we did not trust parts with $\tau_{rr} >> \tau_S$.

7.2 Diode Leakage

As a worst-case approximation, we use the numbers from the spec sheet about leakage current for $V_R = 20V$. This gives $50nA$ of peak typical leakage current.

However, as designed, the V_R of the top diode is equal to the V_R of the bottom diode, so leakage currents will tend to cancel.

Since specs for diode matching were not available, we contacted a device engineer at Texas Instruments who determined typical diode leakage on a wafer. Neither the diodes nor wafer were chosen for any particular reason, other than ready availability. The diodes were the drain and source of 20 mm wide drain extended MOS transistor with 75A gate oxide on two neighboring die. Contacts were made to both sides of the diode only; the remaining pads were floating. The first diode was $20,000\mu m \times 3\mu m$; the second $20,000\mu m\mu m$. The results were as follows ($V_{REV} = -3V$, $t = 100^o$):

Diode	100^o	Diode type
Id11	297pA	$n-/p-$
Id21	298pA	$n-/p-$
Id12	239pA	$n+/p-$
Id22	242pA	$n+/p-$

This gives a match of down to just over 1 percent for the $n-/p-$ diode, and 0.3 percent for the $n+/p-$ diode.

If wafer quality or process quality is worse then this variation could be much larger. However, for a larger geometry device (as we have in the discrete device we are using), or one explicitly designed for matching, we can expect matching to be significantly better. Also, at lower temperatures, we would expect the matching to improve slightly. We can also hand-pick devices to find a particularly well matched pair. Several manufacturers make diodes almost identical to the one used (Fairchild's MMBD1201 series, etc.), so we would hope that at least one of them has a process comparable to TI's.

To be conservative, we decided to arbitrarily state that at least one diode would have matching down to 5 percent. This gives a peak typical leakage of about 2.5nA (if we were not hand-picking parts, this would give a peak maximum leakage of 5nA, since maximum leakage on the spec sheet was twice typical).

To have droop contribute less than a quarter of the final output error, we have $\Delta V = \frac{i}{Ct}$, so $C > \frac{ti}{\Delta V}$. For the high-speed version, this gives $C = 500pf$, while for the high accuracy, $C = 500nf$. Because of charge injection (discussed later), we chose $C = 1nf$ and $C = 1\mu f$ for each version.

7.3 Charge Injection

We can calculate charge injection in one of two ways. First, we can assume that the diodes continue to contact for $\tau_{tt} = 4ns$, which gives a charge injection of $30mA * 4nS = 240pC$ from each diode. This provides an absolute upper bound, and is nowhere close to the real value.

In the second way, we can assume a 6V swing across the 2pf junction capacitance. This gives $12pC$ charge injection, which is closer to the real value, but probably underestimates it by a small bit, since junction capacitance varies with voltage.

Again, we expect charge injection to cancel, since both diodes swing by the same amount. Typical wafer capacitance matching is on the order of $0.1\%/\sqrt{pf}$. We have no idea of how well this will translate to diode capacitance matching. We pulled up a value of 2% matching from Roberge's lecture, so decided to use that number. That brings charge injection bounds down to $4.8pC$ and $240fC$, respectively. We used $480fC$ as a reasonable estimate in between. This gives about $500\mu V$ of charge in the high speed version ($1.9\mu V$ input referred), and negligable injection in the high accuracy version.

Charge injection error will be primarily an offset error, and can largely be canceled out with the offset knob.

7.4 Settling time

For the diode switch to settle to with 0.01% takes about 7 time constants. We have a bias current of 30mA, which gives an on-resistance of 0.83Ω. Hence, our diode switch settling time is $7RC = 6nS$ for the high-speed version and $6\mu S$ for the high accuracy.

7.5 Tracking Error

Our tracking error can be calculated from the error coefficients. Our switch has a transfer function of:

$$\frac{V(o)}{V(i)} = \frac{1}{RCs+1}$$

And an error transfer function of:

$$1 - \frac{1}{RCs+1} = \frac{RCs}{RCs+1}$$

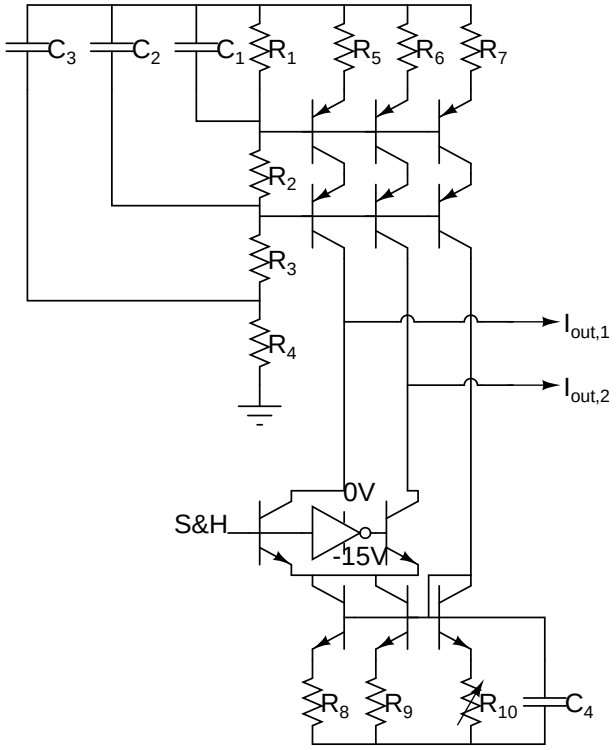
This gives error coefficients of:

$$e_0 = 0, e_1 = RC, e_2 = (RC)^2, e_3 = (RC)^3 ...$$

Our steady state error to a ramp of slope r_t is approximately $RC \cdot 1/r_t$. This comes to about $0.83mV$ for the high speed, and $8.3mV$ for the high accuracy.

7.6 Current Sources and Switch

We have a pair of current sources dumping $30mA$ onto both ends of the diode, and a $60mA$ current drain that we switch between the two diodes. The switching mechanism guarantees that at any point in time, $i_1 = 30 + \alpha \cdot 60mA$, and $i_2 = 30 + (1-\alpha) \cdot 60mA$. Trivially, $i_1 + i_2 = 0$, giving us no switching time error, except due to trivial amounts of charge injection on the switching transistors:



With: $R_2 = R_3 = R_5 = R_6 = R_7 = R_8 = R_9 = R_{10} = 50\Omega$. R_{10} actually consists of a 49Ω in series with a 2Ω pot so we can match currents. $R_1 = 360\Omega$, $R_4 = 9.4k\Omega$, and $C_1 = C_2 = C_3 = 0.1\mu f$.

This gives us negligable switching time error. We use a Philips Semiconductors 74F3037 to drive the inverse transistor. This device has a typical propagation delay of $2nS$ and a maximum of $5.5nS$ when driving a 500Ω $50pF$ load.

Since speed is not an issue on the current sources, we use the exceedingly well matched MAT04 NPN transistor for the current mirror on the bottom, and a pair of moderately well matched that120 quad PNP array for the current sources on top. Since speed is a factor for the cascodes, we use conventional 2N3906 transistors ($\tau_f \approx 300MHz$).

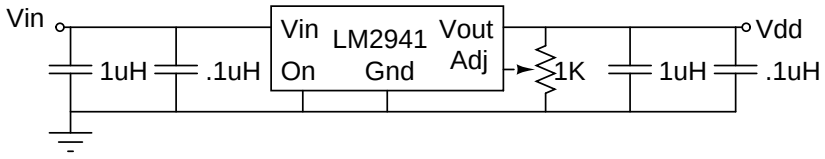
7.7 Current Mismatch Error

We can manually tweak the resistor values to reduce any non-thermal current offset errors.

We have current offsets due to Early effects, as the input moves up and down. The top sources are cascoded directly, while the bottom is effectively cascoded by the sample/hold switch input, giving us a βr_o output impedance, and so current offsets on the order of $\frac{\Delta V}{\beta r_o}$. This will show up as a tiny gain error, and can be partially canceled out with the gain knob. This error is significantly smaller than our accuracy range.

8 Power Supply Rails

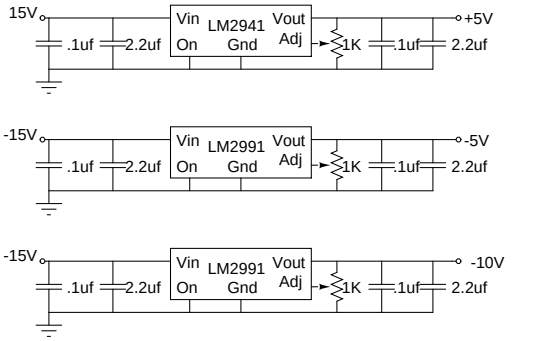
The circuit needs $\pm 5V$ rails for the Burr-Brown parts. To make the positive rails, we use the following regulator circuit:



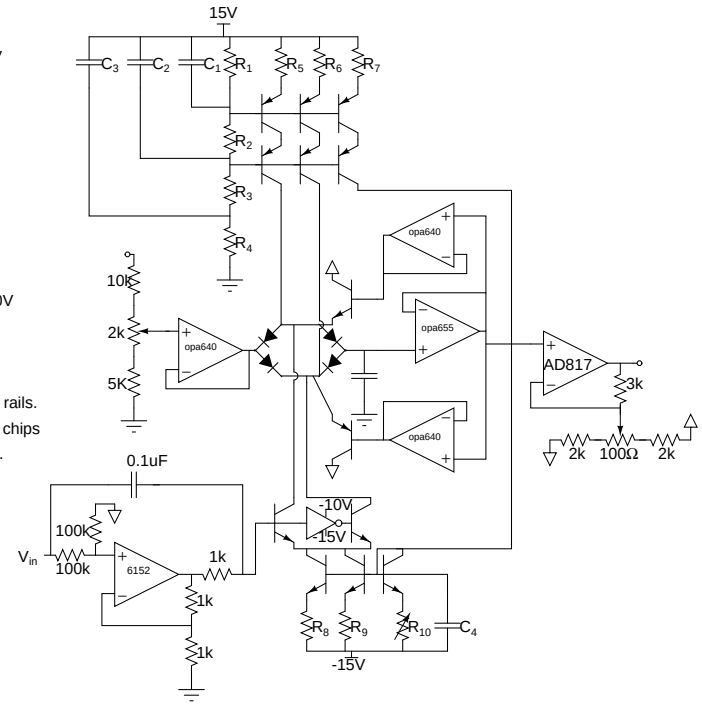
We use an identical circuit with the LM2991 for the negative rails.

9 Conclusion

Our overall schematic is now:



Note: All operational amplifiers except AD817 and lm311 use +/-5V rails. 0.1uF ceramic capacitors should be soldered across the back of all chips between the positive and negative rails for power supply bypassing.



The level-shifting circuit uses a capacitor to pass TTL levels through. The lm356 acts to set the DC level at an appropriate value.

We demonstrated a simple sample-and-hold circuit capable of meeting the basic specs, and capable of operating in either the high-speed or high-accuracy version of the circuit, depending on capacitance. If we add up all errors, our final specs are:

High Speed:

Total Error:	$< 15mV$
Sampling Time (0.01%):	$< 50ns$
For Output to be Ready:	$< 120ns$
Tracking Error:	$< 1mV$

High Accuracy:

Total Error:	$< 15mV$
Sampling Time (0.01%):	$< 7\mu s$
Tracking Error:	$< 10mV$